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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/786,315	IWAKURA ET AL.	
	Examiner	Art Unit	
	Russ Guill	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 June 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to a Request for Continued Examination filed June 3, 2008. No claims were added or canceled. Claims 1 – 38 are pending. Claims 1 – 38 have been examined. Claims 1 – 38 have been rejected.

2. The Examiner would like to thank the Applicant for the well-presented amendment, which was useful in the examination process. The Examiner appreciates the effort to carefully analyze the Office Action, and make appropriate arguments and amendments.

Continued Examination Under 37 CFR 1.114

3. A request for continued examination under 37 CFR 1.114 was filed in this application after appeal to the Board of Patent Appeals and Interferences, but prior to a decision on the appeal. Since this application is eligible for continued examination under 37 CFR 1.114 and the fee set forth in 37 CFR 1.17(e) has been timely paid, the appeal has been withdrawn pursuant to 37 CFR 1.114 and prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on June 3, 3008, has been entered.

Response to Arguments

4. Regarding claims rejected under 35 U.S.C. § 112, first paragraph:
    a. Applicant' arguments have been fully considered, and are persuasive.

5. Regarding claims rejected under 35 U.S.C. § 112, second paragraph:
    a. Applicant' arguments have been fully considered, and are persuasive.

6. Regarding claims 1 - 16, 28 - 37 and 38 rejected under 35 U.S.C. § 101:

a. Applicant's arguments and claim amendments for claims 28 - 37 and 38, and are persuasive.

b. Applicant's arguments and claim amendments for claims 1 – 16 have been fully considered, but are not persuasive, because, while the claims recite a processor in the preamble, the preamble does not have patentable weight. A preamble is generally not accorded any patentable weight where the body of the claim does not depend on the preamble for completeness but, instead, the structural limitations are able to stand alone. [I]t is assumed that the preamble language is duplicative of the language found in the body of the claims or merely provides context for the claims, absent any indication to the contrary in the claims, the specification or the prosecution history.

7. Regarding claims 1, 16, 17, 27, 28 and 38 rejected under 35 U.S.C. § 103:

a. Applicant's arguments and claim amendments have been fully considered, but are not persuasive, as discussed below.

b. The Applicant argues:

c. In the Applicants invention as recited in independent claim 1, as amended, a power supply pair extraction processing section extracts two power supply island patterns as a power supply pair when any two power supply islands existing in two different power supply layers, respectively, in any regions across the entire circuit board, overlap each other, the overlap being determined from the CAD data when any two power supply islands overlap each other, in any regions across the entire circuit board, in plan view from a top side of the circuit board and the patterns of all pairs of overlapping power supply islands across the entire circuit board are extracted by the power supply pair extraction processing section. Thus, in the claimed invention, all areas across the circuit board are considered when the power supply pairs are extracted.

d. In making the rejections of independent claims 1, 17 and 28, the Examiner asserts that Yook teaches all of the features in claims 1, 17 and 28 with the exception of a CAD data obtaining section that obtains CAD data including information concerning a board shape, pattern shapes, and elements; and a CAD data conversion processing section that converts said CAD data into power supply island pattern data, element data, lead pattern data, and via pattern data; from the CAD data. The Examiner asserts that Yook teaches the remaining features of claims 1, 17 and 28 in various sections of pages 66-69 and in Figs. 2 and Fig. 3. See, Office Action, page 11.

e. In making the rejections of independent claims 16, 27 and 38, the Examiner asserts that Yook teaches all of the features in claims 16, 27 and 38 with the exception of a power supply pair extraction processing section that extracts, as a power supply pair, different two power supply layers overlapping each other in a layering direction from data indicative of said circuit board. The Examiner asserts that Yook teaches the remaining features of claims 16, 27 and 38 at page 64, Fig. 2; page 68; Fig. 3; page 64, right- side column, second paragraph that starts with, "The goal of..."; page 67, left-side column, last paragraph, and right-side column, second paragraph that starts with, "For PCB's having..."; and page 68, right-side column. See, Office Action, pp. 13 and 14.

i. The Examiner respectfully replies:

ii. The preceding paragraphs appear to be stating the established facts, and do not appear to need a reply.

f. The Applicant argues:

g. However, the Applicant notes that the cited sections of Yook disclose a method of modeling and analyzing simultaneous switching noise in printed circuit boards using a traditional mesh/SPICE approach and do not disclose or suggest at least the features of a power supply pair extraction processing section that extracts two power supply island patterns as a power supply pair when any two power supply islands existing in two different power supply layers, respectively, in any regions across the circuit board, overlap each other, the overlap being determined from the CAD data when any two power supply islands overlap each other, in any regions across the circuit board, in plan view from a top side of the circuit board and the patterns of all pairs of overlapping power supply islands, across the circuit board, are extracted by the power supply pair extraction processing section, as recited in claim 1, as amended.

i. The Examiner respectfully replies:

ii. Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

iii. However, in order to expedite the examination process, an explanation of how the Yook reference teaches the limitation will be provided.

iv. First, the following principles apply:

(1) *A claimed invention is not patentable if the subject matter of the claimed invention would have been obvious to a person having ordinary skill in the art. KSR International Co. v. Teleflex Inc.*, 127 S. Ct. 1727 (2007).

(2) The question under 35 U.S.C. § 103 is not merely what the references teach but what they would have suggested to one of ordinary skill in the art at the time the invention was made. *In re Lamberti*, 545 F.2d 747, 750 (CCPA 1976).

(3) One of ordinary skill in the art is presumed to have skills apart from what the prior art references expressly disclose. *In re Sovish*, 769 F.2d 738, 742-743 (Fed. Cir. 1985).

(4) A person of ordinary skill is also a person of ordinary creativity, not an automaton. *KSR*, 127 S. Ct. at 1742.

v. The rejection of claim 1 recites the following limitation taught by Yook:

> (1) a power supply pair extraction processing section that extracts two power supply island patterns as a power supply pair when any two power supply islands existing in two different power supply layers, respectively, in any regions across the circuit board, overlap each other, the overlap being determined ~~from the CAD data~~ when any two power supply islands overlap each other, in any regions across the circuit board, in plan view from a top side of the circuit board and the patterns of all pairs of overlapping power supply islands, across the circuit board, are extracted by the power supply pair extraction processing section

vi. Please note that the specification appears to define a power island as a surface pattern and a line pattern of a power supply or GND, as shown for example in figure 2A (page 16, lines 19 – 20), and figure 2A appears to show tiles on the surface of a layer of a printed circuit board as representing a power island.

vii. Next, the Yook reference, page 67, section A. Tiling Procedure, teaches that an entire circuit board is partitioned into a set of tiles. For PCB's (Printed Circuit Board) having multiple power/ground planes, as commonly encountered in high-speed digital circuits, the equivalent circuits for each tile can be stacked vertically to model the 3-D nature of the geometry. Further, the Yook reference, page 68, figure 3, shows a representative printed circuit board in plan view from a top side with at least two overlapping power islands in different locations, and the overlapping power islands are shown as extracted and represented by equivalent circuits. Further, it common knowledge of the ordinary artisan to have a section of a computer program to perform a function (please see, for example, the Harada reference, U.S. Patent Number 6557154, figure 1, that shows program sections, where each section performs a function).

Taken as a whole, these facts would have reasonably suggested the limitation to the ordinary artisan.

viii. Accordingly, the rejection is maintained.

h. The Applicant argues:

i. None of Harada, Shi and Papadopoulou, alone or in any combination thereof, discloses or suggests at least the features of a power supply pair extraction processing section that extracts two power supply island patterns as a power supply pair when any two power supply islands existing in two different power supply layers, respectively, in any regions across the entire circuit board, overlap each other, the overlap being determined from the CAD data when any two power supply islands overlap each other, in any regions across the entire circuit board, in plan view from a top side of the circuit board and the patterns of all pairs of overlapping power supply islands across the entire circuit board are extracted by the power supply pair extraction processing section, as recited in claim 1, as amended.

i. The Examiner respectfully replies:

ii. As discussed above, the Yook reference was relied upon to teach the recited limitation.

j. The Applicant argues:

k. For at least these reasons, the Applicants submit that claim 1 is allowable over the applied art of record. As claim 1 is allowable, the Applicants submit that claims 2 - 15, which depend from allowable claim 1, are likewise allowable for at least the reasons set forth above with respect to claim 1.

i. The Examiner respectfully replies:

ii. As discussed above, the rejection of claim 1 was maintained, and thus, the rejections of the dependent claims are also maintained.

l. The Applicant argues:

m. For similar reasons as those set forth above with respect to claim 1, the Applicants submit that each of independent claims 16, 17, 27, 28 and 38, as amended, are allowable over the applied art of record. As amended claims 17 and 28 are allowable, the Applicant submits that claims 18-26 and 29-37, which depend from allowable claims 17and 28, respectively, are likewise allowable for at least the reasons set forth above with respect to claim 1, 17 and 28.

i. The Examiner respectfully replies:

ii. Since the claims are argued similar to the claims above, please refer to the Examiner's response for the claims above.

Claim Rejections - 35 USC § 101

8. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

9. Claims 1 - 16, 17 - 26, and 27 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

a. Regarding claims 1 and 16 and dependent claims, the claim is directed to a power supply noise analysis model generator. The limitations of the power supply noise analysis model generator appear to allow an interpretation that is entirely software. The processing sections claimed in the limitations appear to be entirely software. Further, the claim does not appear to have a processor that is functionally connected to the processing sections to allow any functionality to be realized.

i. While the claims recite a processor in the preamble, the preamble does not have patentable weight. A preamble is generally not accorded any patentable weight where the body of the claim does not depend on

> the preamble for completeness but, instead, the structural limitations are able to stand alone. [I]t is assumed that the preamble language is duplicative of the language found in the body of the claims or merely provides context for the claims, absent any indication to the contrary in the claims, the specification or the prosecution history.

b. Regarding claims 17 and 27, the claim is directed to a power supply noise analysis model generation method. A valid process under 35 USC § 101 must either 1) transform underlying subject matter, or 2) be tied to another statutory class, such as a *particular apparatus*. In order to qualify as a statutory process, the claim should positively recite the other statutory class to which it is tied, for example by identifying the apparatus that accomplishes the method steps. A mere recitation of a computer in the preamble does not appear to be sufficient to tie the process to a particular apparatus.

c. Dependent claims inherit the defects of the parent claims.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under

37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

12. **Claims 1 - 7, 13 - 14, 16 - 23, 27 – 34 and 38** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yook (Jong-Kwan Yook et al.; "Computation of Switching Noise in Printed Circuit Boards", 1997, IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part A, Volume 20, Number 1, March 1997, pages 64 - 75) in view of Harada (U.S. Patent Number 6,557,154).

a. The art of Yook is directed to computation of switching noise in printed circuit boards (*page 64, Title*).

b. The art of Harada is directed to analysis of the electromagnetic characteristics of a printed circuit board (*Abstract*).

c. The art of Yook and the art of Harada are analogous art because they are both directed to the analysis of electromagnetic characteristics of a printed circuit board.

d. Regarding **claims 1, 17, 28**:

e. Yook appears to teach:

f. a power supply pair extraction processing section that extracts two power supply island patterns as a power supply pair when any two power supply islands existing in two different power supply layers, respectively, in any regions across the entire circuit board, overlap each other, the overlap being determined ~~from the CAD data~~ when any two power supply islands overlap each other, in any regions across the entire circuit board, in plan view from a top side of the circuit board and the patterns of all pairs of overlapping power supply islands across the entire circuit board are extracted by the power supply pair extraction processing section (*page 68, figure 3, please note the*

multiple power supply islands extracted from the PCB; and page 67, left-side column, last paragraph, and right-side column, second paragraph that starts with, "For PCB's having . . ."; the limitation would have been obvious in view of the knowledge of the ordinary artisan as described in the references listed in the Conclusion section of this Office Action);

g. a node layout processing section that positions plural nodes on a power supply pair region which is occupied by each power supply pair on a plane of said circuit board (*page 67, left-side column, section A. Tiling Procedure, first paragraph*);

h. a node region determination processing section that determines node regions surrounding said nodes, respectively (*page 67, left-side column, section A. Tiling Procedure, first paragraph*);

i. an impedance parameter determination processing section that determines impedance parameters expressing relationships between said nodes, respectively (*pages 67 - 69, section B. Equivalent Circuits; and page 66, figure 2*);

j. a power supply layer model generation processing section that connects said nodes to each other using said impedance parameters, to generate a power supply layer model (*page 66, figure 2, PCB Lumped Electrical Ckt Model; page 68, figure 3, circuits displayed in the lower right corner and upper right corner*);

k. a power supply noise analysis model generation processing section that connects said power supply layer model, said lead pattern data and said via pattern data to one another to generate a power supply noise analysis model supplied to a user by said power supply noise analysis model generator (*page 66, figure 2, PCB Lumped Electrical Ckt Model; page 68, figure 3, circuits displayed in the lower right corner and upper right corner; page 68, right-side column, section 2) Power/Signal/Ground Tiles, teaches lead pattern data; page 64, right-side column, second paragraph that starts with, "The goal of . . .", "PCB tile models are subsequently combined with models for chip current drivers and package leads to produce an electrical simulation model"; page 67, section A. Tiling Procedure, first paragraph; page 69, section*

3) Power/Ground Pin Tiles, first paragraph; page 66, left-side column, last paragraph, first sentence);

l. Yook does not specifically teach:

m. a CAD data obtaining section that obtains CAD data for the circuit board including information concerning a board shape, pattern shapes, and elements;

n. a CAD data conversion processing section that converts said CAD for the circuit board data into power supply island pattern data, element data, lead pattern data, and via pattern data;

o. ~~the overlap being determined~~ from the CAD data;

p. Harada appears to teach:

q. a CAD data obtaining section that obtains CAD data for the circuit board including information concerning a board shape, pattern shapes, and elements (*figure 34, block labeled "CAD for layout of PCB"; and figure 33; and column 4, lines 6 - 17*);

r. a CAD data conversion processing section that converts said CAD for the circuit board data into power supply island pattern data, element data, lead pattern data, and via pattern data (*figure 34, block labeled "CAD for layout of PCB"; and figure 33; and column 4, lines 6 - 17; since the input information about ICs is used to build a circuit model, it would have been obvious that data conversion is performed that converts CAD data into power supply island pattern data, element data, lead pattern data, and via pattern data*);

s. the CAD data (*figure 34, block labeled "CAD for layout of PCB"*);

t. The motivation to use the art of Harada with the art of Yook would have been the benefit recited in Harada that the invention is a PCB design method that reduces radiation of electromagnetic waves by optimizing layout of a substrate (*Abstract, first sentence*), which would have been recognized as a benefit by the ordinary artisan.

u. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Harada with the art of Yook to produce the claimed invention.

v. Regarding **claims 16, 27, 38:**

w. Yook appears to teach:

x. a power supply pair extraction processing section that extracts, as power supply pairs, all of any two different power supply layers located in any regions across the entire circuit board, that overlap each other in a plan view from a top side of the circuit board, said overlap being determined from data indicative of said circuit board (*page 68, figure 3, please note the multiple power supply islands extracted from the PCB; and page 67, left-side column, last paragraph, and right-side column, second paragraph that starts with, "For PCB's having . . ."*);

y. a power supply noise analysis model generation processing section that uses said power supply pairs extracted to generate a power supply noise analysis model (*page 66, figure 2, PCB Lumped Electrical Ckt Model; page 68, figure 3, circuits displayed in the lower right corner and upper right corner; page 68, right-side column, section 2) Power/Signal/Ground Tiles, teaches lead pattern data; page 64, right-side column, second paragraph that starts with, "The goal of . . .", "PCB tile models are subsequently combined with models for chip current drivers and package leads to produce an electrical simulation model"; page 67, section A. Tiling Procedure, first paragraph; page 69, section 3) Power/Ground Pin Tiles, first paragraph; page 66, left-side column, last paragraph, first sentence*);

z. Yook does not specifically teach (in ***bold italic underline***):

aa. a power supply pair extraction processing section that extracts, as a power supply pair, different two power supply layers overlapping each other in a layering direction ***from data indicative of said circuit board***;

bb. Harada appears to teach:

cc. data indicative of said circuit board (*figure 34, block labeled "CAD for layout of PCB"; and figure 33; and column 4, lines 6 - 17*);

dd. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Harada with the art of Yook to produce the claimed invention.

ee. Regarding **claims 2, 18, 29**:

ff. Yook appears to teach:

gg. said impedance parameters are a reactance L, a resistance R, and an interlayer capacitance C (*page 68, figure 3, circuit diagram in the upper right corner with L, C and R elements*).

hh. Regarding **claims 3, 19, 30**:

ii. Yook appears to teach:

jj. wherein if a power supply pair space sandwiched between power supplies of an observed power supply pair is contacted or overlapped by another power supply pair space of any other power supply pair, said power supply pair extraction processing section makes said observed power supply pair and said other power supply pair into a group (*page 68, figure 3, the models in the lower half of the figure; it would have been obvious to group overlapping planes*).

kk. Regarding **claims 4, 20, 31**:

ll. Yook does not specifically teach:

mm. a ripple processing section that positions, on said power supply pair region, ripples which are wave fronts of electromagnetic waves radiated into said power supply pair region from said elements, wherein

said node layout processing section positions said nodes, based on pitches of said ripples.

nn. Harada appears to teach:

oo. a ripple processing section that positions, on said power supply pair region, ripples which are wave fronts of electromagnetic waves radiated into said power supply pair region from said elements, wherein said node layout processing section positions said nodes, based on pitches of said ripples (*column 15, lines 34 - 67, and column 16, lines 1 - 67*).

pp. Regarding **claims 5, 21, 32:**

qq. Yook does not specifically teach:

rr. said ripple processing section uses rising or failing times of those of said elements which are mounted on said power supply pair region, maximum operating frequencies of those elements, and areas of said ripples, to calculate intervals between said ripples.

ss. Harada appears to teach:

tt. said ripple processing section uses rising or failing times of those of said elements which are mounted on said power supply pair region, maximum operating frequencies of those elements, and areas of said ripples, to calculate intervals between said ripples (*column 15, lines 34 - 67, and column 16, lines 1 - 67*).

uu. Regarding **claims 6, 22, 33:**

vv. Yook does not specifically teach:

ww. said ripple processing section spreads said ripples into power supply pair regions of power supply pairs which belong to a group.

xx. Harada appears to teach:

yy. said ripple processing section spreads said ripples into power supply pair regions of power supply pairs which belong to a group (*column 15, lines 34 - 67, and column 16, lines 1 - 67*).

zz. Regarding **claim 7, 23, 34**:

aaa. Yook does not specifically teach:

bbb. a ripple display processing section that searches for outline coordinates of said ripples, and displays said ripples with the use of said outline coordinates.

ccc. Harada appears to teach:

ddd. a ripple display processing section that searches for outline coordinates of said ripples, and displays said ripples with the use of said outline coordinates (*figure 23, element 65*).

eee. Regarding **claim 13**:

fff. Yook appears to teach:

ggg. said impedance parameter determination processing section determines a reactance L based on distances between said nodes, and determines an interlayer capacitance C with the use of the areas of said node regions and a distance or distances between power supply layers, and said power supply layer model generation processing section arranges said reactance L and said resistance R between nodes on an upper surface of each power supply pair and between nodes on a lower surface of each power supply pair, and arranges each interlayer capacitance C between such a couple of nodes that are arranged at equal positions respectively on the upper and lower surfaces of said power supply pair (*page 68, figure 3; and page 68, left-side column, equations 6, 7, 8*).

hhh. Yook does not specifically teach (in ***bold underline italic***):

iii. said impedance parameter determination processing section determines a reactance L ***and a resistance R*** based on distances between said nodes, and determines an interlayer capacitance C with the use of the areas of said node regions and a distance or distances between power supply layers, and said power supply layer model generation processing section arranges said reactance L and said resistance R between nodes on an upper surface of each power supply pair and between nodes on a lower surface of each power supply pair, and arranges each interlayer

capacitance C between such a couple of nodes that are arranged at equal positions respectively on the upper and lower surfaces of said power supply pair.

jjj. Harada appears to teach:

kkk. said impedance parameter determination processing section determines ***a resistance R*** based on distances between said nodes (*column 18, lines 1 - 14*).

lll. Regarding **claim 14**:

mmm. Yook appears to teach:

nnn. a power supply noise analysis model storage that stores said power supply noise analysis model (*page 66, figure 2; since the method is implemented on a computer, it would have been obvious that the PCB Lumped Electrical Ckt Model was stored in storage*).

13. **Claims 8 - 10, 24 - 26, 35 - 37 and 15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yook as modified by Harada as applied to claims **1 - 7, 13 - 14, 16 - 23, 27 - 34 and 38** above, and further in view of Shi (Hao Shi et al.; "Modeling Multilayered PCB Power-Bus Designs Using an MPIE Based Circuit Extraction Technique", August 1998, IEEE International Symposium on Electromagnetic Compatibility, pages 647 - 651).

a. Yook as modified by Harada teaches a power supply noise analysis model, as recited in claims **1 - 7, 13 - 14, 16 - 23, 27 - 34 and 38** above.

b. The art of Shi is directed to generating a SPICE model of a PCB and integrating it with IC device models and PCB trace models (*page 651, section Conclusion*).

c. The art of Shi and the art of Yook as modified by Harada are analogous art because they are both directed to the analysis of electromagnetic characteristics of a printed circuit board.

d. **Regarding claims 8, 24, 35**:

e. Yook as modified by Harada does not specifically teach:

f. a mesh division processing section that divides said power supply pair region with the use of meshes based on a wavelength of one of said elements that is mounted on said power supply pair region of the circuit board that has the highest operating frequency.

g. Shi appears to teach:

h. a mesh division processing section that divides said power supply pair region with the use of meshes based on a wavelength of one of said elements that is mounted on said power supply pair region of the circuit board that has the highest operating frequency (*page 647, section III. PCB power-bus analysis using CEMPIE, second paragraph, an upper frequency is used to determine the mesh size*).

i. The motivation to use the art of Shi with the art of Yook as modified by Harada would have been the advantage recited in Shi that the formulation starts from first principles and incorporates the distributed behavior of the planes, yet does not solve the discretized integral equations, rather, extracts an equivalent circuit model (*page 651, section V. Conclusion*), which would have been recognized as a benefit by the ordinary artisan to save time.

j. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Shi with the art of Yook as modified by Harada to produce the claimed invention.

k. Regarding **claim 9, 25, 36**:

l. Yook as modified by Harada does not specifically teach:

m. an internal data storage which stores information for every of said meshes into a table on which coordinates on said circuit board correspond to addresses.

n. Shi appears to teach:

o. an internal data storage which stores information for every of said meshes into a table on which coordinates on said circuit board correspond to addresses (*page 648, figure 1, and Table I; since the meshes are implemented on a computer, it would have been obvious that there was an internal data storage which stores information for every of said meshes into a table on which coordinates on said circuit board correspond to addresses*).

p. Regarding **claim 10, 26, 37**:

q. Yook as modified by Harada does not specifically teach:

r. the information for every of said meshes includes at least one of a ripple level which indicates the number of ripples from an element to a corresponding mesh, the presence or absence of a node in said corresponding mesh, and a node region identifier expressing a node region to which said corresponding mesh belongs.

s. Shi appears to teach:

t. the information for every of said meshes includes at least a node region identifier expressing a node region to which said corresponding mesh belongs (*page 648, figure 1 and figure 2; the node regions are labeled power-bus and power-island, and it would have been obvious that each node had a node region identifier to identify the node region*).

u. Regarding **claim 15**:

v. Yook as modified by Harada does not specifically teach:

w. said power supply noise analysis model generation processing section further generates a total circuit model in which said power supply

noise analysis model is connected to said element data, and stores said total circuit model into said power supply noise analysis model storage.

x. Shi appears to teach:

y. said power supply noise analysis model generation processing section further generates a total circuit model in which said power supply noise analysis model is connected to said element data, and stores said total circuit model into said power supply noise analysis model storage (*page 651, section V. Conclusion; since the method is implemented in a computer, it would have been obvious that the model was stored for analysis*).

14. **Claims 11 - 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yook as modified by Harada as applied to claims **1 - 7, 13 - 14, 16 - 23, 27 - 34 and 38** above, and further in view of Papadopoulou (U.S. Patent Number 6,178,539).

a. Yook as modified by Harada teaches a power supply noise analysis model, as recited in claims **1 - 7, 13 - 14, 16 - 23, 27 - 34 and 38** above.

b. The art of Papadopoulou is directed to calculating critical areas of circuit layouts using Voronoi diagrams (*Abstract*).

c. The art of Papadopoulou and the art of Yook as modified by Harada are analogous art because they are both contain the art of tiling a circuit (*Papadopoulou, Abstract, Voronoi diagram; Yook, page 66, figure 2, tiling processor*).

d. **Regarding claims 11**:

e. Yook as modified by Harada does not specifically teach:

f. wherein, taking a most adjacent node as the node closest to an observed node within a sector having a predetermined radius about said observed node as the center of said sector, said node region determination processing section searches for adjacent nodes by rotating said sector about said observed node.

g. Papadopoulou appears to teach:

h. wherein, taking a most adjacent node as the node closest to an observed node within a sector having a predetermined radius about said observed node as the center of said sector, said node region determination processing section searches for adjacent nodes by rotating said sector about said observed node (*column 5, lines 19 - 67, column 6, lines 1 - 9; it would have been obvious in computing a Voronoi tessellation to search for adjacent nodes by rotating a sector about an observed node*).

i. **Regarding claim 12:**

j. Yook as modified by Harada does not specifically teach:

k. wherein said node region determination processing section removes a square from said power supply pair region thereby to determine an edge of the node region of said observed node with respect to said most adjacent node, said square having as an edge a perpendicular bisector of a predetermined length between said observed node and said most adjacent node and containing said most adjacent node, so that edges of said node region of said observed node are sequentially determined with respect to all the adjacent nodes, respectively, in the order of increasing distance from said most adjacent node, finally to determine the node region of said observed node.

l. Papadopoulou appears to teach:

m. wherein said node region determination processing section removes a square from said power supply pair region thereby to determine an edge of the node region of said observed node with respect to said most adjacent node, said square having as an edge a perpendicular bisector of a predetermined length between said observed node and said most adjacent node and containing said most adjacent node, so that edges of said node region of said observed node are sequentially determined with respect to all the adjacent nodes, respectively, in the order of increasing distance from said most adjacent node, finally to determine the node region of said observed node (*column 5, lines 19 - 67, column*

6, lines 1 - 9; it would have been obvious in computing a Voronoi tessellation to perform the limitation) .

n. The motivation to use the art of Papdopoulou with the art of Yook as modified by Harada would have been the benefit recited in Papadopoulou that in particularly useful methods, the step of decomposing each region into shapes is preferably included (*column 3, lines 5 – 8*).

o. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Papdopoulou with the art of Yook as modified by Harada to produce the claimed invention.

15. **Examiner's Note:** Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the Applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner. *The entire reference is considered to provide disclosure relating to the claimed invention.*

Conclusion

16. The prior art made of record in a previous Office action is used to show knowledge of the ordinary artisan:

a. Novak (U.S. Patent Number 7,277,841) teaches a method of modeling power and ground planes.

b. Mabuchi (U.S. Patent Application Publication 2003/0109995) teaches generating a SPICE model of a printed circuit board.

c. Frank Y. Yuan, "Electromagnetic Modeling and Signal Integrity Simulation of Power/Ground Networks in High Speed Digital Packages and Printed Circuit Boards", 1998, Proceedings of the 1998 Design Automation Conference, pages 421 – 426; teaches power/ground supply networks involve complex, large structures such as combinations of plane/partial planes, and integrating the PCB model with the circuit model.

d. S. Luan et al.; "Extracting CAD Models for Quantifying Noise Coupling between Vias in PCB Layouts", 28 May 2002, Proceedings of the 52nd Electronic Components and Technology Conference, pages 343 – 346; teaches extracting printed circuit board parameters from CAD, generating a SPICE model of the printed circuit board, and integrating the board model with the circuit model for analysis.

e. Albert E. Ruehli et al.; "Progress in the Methodologies for the Electrical Modeling of Interconnects and Electronic Packages", May 2001, Proceedings of the IEEE, Volume 89, Number 5, pages 740 – 771; teaches extracting CAD data to generate a SPICE model.

f. Hayashi (U.S. Patent Number 6,842,727) teaches extracting layout data, and generating a SPICE model.

g. Du Cloux (U.S. Patent Number 5,625,578) teaches meshing a printed circuit board to generate an equivalent circuit.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Russ Guill whose telephone number is 571-272-7955. The examiner can normally be reached on Monday – Friday 9:30 AM – 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Any

inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group Receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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